(54)[Title of the Invention]

PHOTOELECTRIC CONVERSION APPARATUS, SOLID-STATE IMAGE PICKUP APPARATUS AND SYSTEM

[Claims for the Patent]

[Claim 1]

A photoelectric conversion apparatus including pixels arranged thereon, which convert optical signals to electric signals to generate amplification signals based on the electric signals, characterized by comprising:

an amplifier to amplify at least an amplification signal superimposed with noise signals generated when potentials of the pixels are reset and removing means that removes the noise signals or the offset of the amplifier.

[Claim 2]

The photoelectric conversion apparatus according to claim 1, characterized in that the amplifier is provided between the pixels and the removing means.

[Claim 3]

The photoelectric conversion apparatus according to claim 1 or claim 2, characterized in that the removing means comprises a first capacitor in which the noise signals and the offset of the amplifier are stored; a second capacitor in which the noise signals, the offset of the amplifier and the output signals of the amplifier are stored; and differential means that carries out differentiation of the respective signals held in the first and the second capacitors.

[Claim 4]

The photoelectric conversion apparatus according to claim 1 or 2, characterized in that the removing means comprises clamp means that clamps the noise signals and a capacitor which holds a clamp potential by the clamp means and holds an output of the amplifier.

[Claim 5]

A photoelectric conversion apparatus including pixels

arranged thereon, which convert optical signals to electric signals to generate amplification signals based on the electric signals, characterized by comprising:

an amplifier to amplify at least an amplification signal output from the pixels; applying means that applies a clamp potential to the amplifier at the time the noise signals generated when potentials of the pixels are reset are output from the pixels; a first capacitor in which an offset of the amplifier is stored; a second capacitor in which the offset of the amplifier and an output of the amplifier are stored; and differential means that carries out differentiation of the respective signals held in the first and the second capacitors.

[Claim 6]

The photoelectric conversion apparatus according to claim 5, characterized in that the amplifier is provided in a transmission line for the amplification signal.

[Claim 7]

The photoelectric conversion apparatus according to any one of claims 1 to 6, characterized in that the amplifier comprises a differential input stage which operates at a constant current and a source follower or an emitter follower which operates at a constant current.

[Claim 8]

The photoelectric conversion apparatus according to any one of claims 1 to 7, characterized in that the gain of the amplifier is determined by capacitor ratio of a plurality of capacitors which the amplifier comprises.

[Claim 9]

The photoelectric conversion apparatus according to any one of claims 1 to 8, characterized in that the amplifier comprises a capacitor having one electrode connected to a differential input stage and the other electrode connected to a predetermined potential and a capacitor having one electrode connected to a differential input stage and the other electrode connected to a source follower or an emitter follower.

[Claim 10]

A solid-state image pickup apparatus characterized by comprising the photoelectric conversion apparatus according to

any one of claims 1 to 9.

[Claim 11]

The solid-state image pickup system characterized by comprising the solid-state image pickup apparatus according to claim 10.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a photoelectric conversion apparatus, a solid-state image pickup apparatus and a system and, in particular, relates to a photoelectric conversion apparatus, a solid-state image pickup apparatus and a system such as a digital camera.

[0002]

[Conventional Art]

Conventionally, a CCD image pickup device is frequently used as the solid-state image pickup apparatus due to its good signal-to-noise ratio. However, on the other hand, so-called amplification-type solid-state image pickup apparatus, which is advantageous for convenience in use and small power consumption, has been developed.

[0003]

An amplification-type solid-state image pickup apparatus converts optical signals to electric signals with a photoelectric conversion device such as a photodiode, guides the electric signals to a control electrode of a transistor to output amplification signals based on electric signals from a main electrode of the transistor, and includes an SIT image sensor with an SIT as amplification transistor (A. Yusa, J. Nishizawa et al., "SIT image sensor: Design consideration and characteristics," IEEE trans. Vol. ED-33, pp.735-742, June 1986.), a BASIS with a bipolar transistor (N. Tanaka et al., "A 310K pixel bipolar imager (BASIS)," IEEE Trans. Electron Devices, vol. 35, pp. 646-652, may 1990), a CMD with a JFET including a control electrode being depleted (Nakamura et al., "Gate-stored MOS phototransistor image sensor", in The Journal of the Institute of Television Engineers of Japan, 41, 11, pp. 1075-1082 Nov. 1987), a CMOS sensor with a MOS transistor (S. K. Mendis, S.E. Kameny and E.R. Fossum, "A 128 x 128 CMOS active image sensor for highly integrated imaging systems," in

IEDM Tech. Dig., 1993, pp. 583-586.) and the like.
[0004]

In particular, a CMOS sensor matches with a CMOS process well and allows production of on-chip peripheral CMOS circuit and therefore a lot of efforts are exerted for its development. However, a common disadvantage of those amplification-type solid-state image pickup apparatuses is that signals of the image sensor carry fixed pattern noise (FPN) since the output offset of the amplification transistor provided in each pixel is different one from the other. In order to remove that FPN, various signal readout circuits have been conventionally devised. But here, a representative example of the CMOS sensor will be described below.
[0005]

Figure 8 is a circuit diagram illustrating a conventional CMOS image sensor. Figure 8 includes pixels 1, a photodiode 2 which converts an optical signal to an electric signal for storage, a transfer MOS transistor 4 which transfers electric signals stored in the photodiode 2, an amplification MOS transistor 3 which amplifies optical signals transferred from the photodiode 2, a reset MOS transistor 5 which resets gate electrode potential of the amplification MOS transistor 3, a power potential supply line 6 which is connected to the drain electrode of the reset MOS transistor 5 and the drain electrode of the amplification MOS transistor 3 and supplies the side of the pixels 1 with power potential, a selection switch MOS transistor 7 which selects a pixel 1 of an output source of amplification signals based on electric signals, a signal output line 8 which transmits amplification signals and a constant current supply MOS transistor 9 for supplying a vertical output line 8 with a constant current.
[0006]

In addition, there are included a reset control line 10 for controlling the gate potential of the reset MOS transistor 5, a transfer control line 11 for controlling the gate potential of the transfer MOS transistor 4, a selection control line 12 for controlling the gate potential of the selection MOS transistor 7 and a constant potential supply line 13 for supplying a constant potential to the gate of the MOS transistor 9 such that the MOS transistor 9 performs a

saturation region operation to serve as a constant current supply source.

[0007]

Moreover, there are included a pulse terminal 14 for supplying a reset pulse to the reset control line 11, a pulse terminal 15 for supplying a transfer pulse to the transfer control line 10, a pulse terminal 16 supplies a selection pulse to the selection control line 12, a vertical scanning circuit 17 for sequentially selecting and scanning the rows of pixels 1 arrayed in a matrix, a first row selection output line 18-1 and a second row selection output line 18-2 of the vertical scanning circuit, a switch MOS transistor 19 which leads a pulse from the pulse terminal 15 to the reset control line 10, a switch MOS transistor 20 which leads a pulse from the pulse terminal 14 to the transfer control line 11 and a switch MOS transistor 21 for supplying a pulse from the pulse terminal 16 to the selection control line 12.

[0008]

Further, there are included a readout circuit 22 which reads out a signal from the pixel 1, a capacitor 23 which holds a reset signal output from the pixel 1, a capacitor 24 which holds an optical signal output from the pixel 1, a switch MOS transistor 25 which controls conduction between the vertical output line 8 and the capacitor 23, a switch MOS transistor 26 which controls conduction between the vertical output line 8 and the capacitor 24, pulse supply terminals 37 and 38 which apply pulses to the gates of the switch MOS transistors 25 and 26, respectively, a horizontal output line 27 to which a noise signal held in the capacitor 23 is transmitted, a horizontal output line 28 which transmits an optical signal held in the capacitor 24, a switch MOS transistor 29 which controls conduction between the capacitor 23 and the horizontal output line 27 and a switch MOS transistor 30 which controls conduction between the capacitor 24 and the signal output line 28.

[0009]

In addition, there are included a horizontal output line reset MOS transistor 31 which resets the potential of the horizontal output line 27, a horizontal output line reset MOS transistor 32 which resets the potential of the horizontal

output line 28, a power supply terminal 33 which supplies a reset potential to the source electrodes of the horizontal output line reset MOS transistors 31 and 32, a horizontal scanning circuit 34 which sequentially selects the capacitors 23 and 24 which are provided for each column of the pixels 1 arrayed in a matrix, 35-1 and 35-2 connected to the switch MOS transistors 29 and 30, a pulse supply terminal 36 which applies a pulse to the gates of the horizontal output line reset MOS transistors 31 and 32, a differential amplifier 39 which amplifies and outputs the voltage difference between the potential of the horizontal output line 27 and that of the signal output line 28 and an output terminal 40 of the differential amplifier 39.

[0010]

Here, Figure 8 illustrates 2-row 2-column pixels 1 for the sake of simplification. However, in practice, the matrix number will correspond with an intended use.

[0011]

Figure 9 includes timing charts illustrating operation of the circuit in Figure 8. Here, the MOS transistors illustrated in Figure 8 are all N types, which are turned on when the gate potential is at high level and off at low level. At first, when a pulse signal applied to the first row selection output line 18-1 by the vertical scanning circuit 17 is switched to high level, the operation of the pixels 1 on the first row will become feasible. When the pulse signal applied to the pulse terminal 16 is switched to high level, the source of the amplification MOS transistor 3 of the pixel 1 and the constant current supply MOS transistor 9 are brought into connection and output of the signal from the side of the pixel 1 to the vertical output line 8 will become feasible.

[0012]

By switching the pulse signal applied to the pulse terminal 15 to high level, the reset MOS transistor 5 is turned on and the gate part of the amplification MOS transistor 3 is reset to a reset potential.

[0013]

Next, a pulse applied to the pulse supply terminal 37 is switched to high level. The output signal of the pixel 1 is read out and stored in the capacitor 23 through the MOS

transistor 25.
[0014]

Next, by switching a pulse applied to the pulse terminal 14 to high level, optical signals generated in the photodiode 2 are transferred to the gate of the MOS transistor 3 through the transfer MOS transistor 4.
[0015]

Here, a noise signal occurring at the time of resetting the potential of the pixel 1 is superimposed onto the optical signal transferred to the gate of the MOS transistor 3.
[0016]

Subsequently, when a high level pulse is applied to the pulse supply terminal 38, an amplification signal based on an optical signal on which a noise signal is superimposed is stored in the capacitor 24 through the MOS transistor 26.
[0017]

When the horizontal scanning circuit 34 is driven, the pulse signals output to the first column selection output line 35-1 and a second column selection output line 35-2 sequentially get to high level. The signals stored in the capacitors 23 and 24 are output to the horizontal output lines 27 and 28 through the MOS transistors 29 and 30 respectively.
[0018]

Before the high level pulses are output to the first column selection output line 35-1 and the second column selection output line 35-2, it is necessary that the pulse applied to the pulse supply terminal 36 is set at high level to reset the potential of the horizontal output lines 27 and 28 through the horizontal output line reset MOS transistors 31 and 32 in advance.
[0019]

Respective signals lead to the horizontal output lines 27 and 28 are input to the differential amplifier 39 so that the difference is taken and the amplification signal based on an optical signal is output from the output terminal 40.
[0020]

Similarly, if signals are read out from the pixels 1 in the second row, amplification signals based on the optical signals are output from the output terminal 40.
[0021]

[Problems to be Solved by the Invention]

However, the conventional techniques have the following problems. That is, noise cannot be removed completely since there is a little difference in the gain of signals input to the differential amplifier as described below.

[0022]

With the capacitors 23 and 24 being CTN and CTS respectively and capacitors of the horizontal output lines 27 and 28 being CHN and CHS respectively, the gains up to the differential amplifier 39 are respectively

CTN/(CTN+CHN)

CTS/(CTS+CHS).

[0023]

In the designing stage, the both gains are made equal under the conditions of:

CTN=CTS

CHN=CHS.

However, actually the gains of the two routes are a little different since it is difficult to form two output routes with the same layout and a displacement from the design occurs in an actual processing step.

[0024]

Due to the reasons described above, the residual after removing dispersion in the noise signals of the pixels appears as so-called fixed pattern noise (FPN) and the signal-to-noise ratio of the pixels does not increase sufficiently.

[0025]

In addition, a gain of the signal output up to the differential amplifier 39 drops. That is, the signal voltage input to the differential amplifier is smaller than the pixel output voltage by the portion of the gain being:

CTS/(CTS+CHS)<1.

[0026]

On the other hand, the differential amplifier 39 always generates some random noise. In addition, thermal noise originated from storage capacitors 23 and 24 up to the differential amplifier 39 and parasitic capacitors of the horizontal output lines 27 and 28 occurs. Thereby, the signal-to-noise ratio of the sensor on the random noise will drop.

[0027]

Therefore, an object of the present invention is to reduce FPN and to improve the signal-to-noise ratio.

[0028]

In addition, an object of the present invention is to reduce random noise and to improve the signal-to-noise ratio.

[0029]

[Means for solving the Problems]

In order to solve the above described problems, there is provided a photoelectric conversion apparatus including pixels arranged thereon, which convert optical signals to electric signals to generate amplification signals based on the electric signals, characterized by comprising an amplifier to amplify at least an amplification signal superimposed with noise signals generated when potentials of the pixels are reset and removing means which removes the noise signals or the offset of the amplifier.

[0030]

In addition, the present invention is a photoelectric conversion apparatus including pixels arranged thereon, which convert optical signals to electric signals to generate amplification signals based on the electric signals, characterized by comprising an amplifier to amplify at least the amplification signal output from the pixels; applying means that applies a clamp potential to the amplifier at the time the noise signals generated when potentials of the pixels are reset are output from the pixels; a first capacitor in which an offset of the amplifier is stored; a second capacitor in which the offset of the amplifier and an output of the amplifier are stored; and differential means that carries out differentiation of the respective signals held in the first and the second capacitors.

[0031]

Moreover, a solid-state image pickup apparatus of the present invention comprises the photoelectric conversion apparatus.

[0032]

Further, the solid-state image pickup system comprises the solid-state image pickup apparatus.

[0033]

[Embodiments of the Invention]

(Embodiment 1)

Figure 1 is an equivalent circuit diagram of a solid-state image pickup apparatus of an embodiment 1 of the present invention. Figure 1 includes pixels 1, a photodiode 2 which converts an optical signal to an electric signal for storage, a transfer MOS transistor 4 which transfers electric signal stored in the photodiode 2, an amplification MOS transistor 3 which amplifies electrical signals transferred from the photodiode 2, a reset MOS transistor 5 which resets the potential of the gate electrode and the like of the amplification MOS transistor 3, a power potential supply line 6 which is connected to the drain electrode of the reset MOS transistor 5 and the drain electrode of the amplification MOS transistor 3 and supplies the pixels 1 with power potential, a selection switch MOS transistor 7 which selects a pixel 1 of an output source of amplification signals based on electric signals, a vertical output line 8 which transmits amplification signals and a constant current supply MOS transistor 9 for supplying a vertical output line 8 with a constant current.

[0034]

In addition, there are included a reset control line 10 for controlling the gate potential of the reset MOS transistor 5, a transfer control line 11 for controlling the gate potential of the transfer MOS transistor 4, a selection control line 12 for controlling the gate potential of the selection MOS transistor 7 and a constant potential supply line 13 for supplying a constant potential to the gate of the MOS transistor 9 such that the MOS transistor 9 performs a saturation region operation to serve as a constant current supply source.

[0035]

Moreover, there are included a pulse terminal 14 for supplying a reset pulse to the reset control line 11, a pulse terminal 15 for supplying a transfer pulse to the transfer control line 10, a pulse terminal 16 for supplying a selection pulse to the selection control line 12, a vertical scanning circuit 17 which sequentially selects and scans the rows of pixels 1, a first row selection output line 18-1 and a second row selection output line 18-2 of the vertical scanning

circuit 17, a switch MOS transistor 19 which leads a pulse from the pulse terminal 15 to the reset control line 10, a switch MOS transistor 20 which leads a pulse from the pulse terminal 14 to the transfer control line 11 and a switch MOS transistor 21 for supplying a pulse from the pulse terminal 16 to the selection control line 12.

[0036]

In addition, there are included a gain amplifier 41 which is provided in each column and amplifies respective signals from the pixels 1, a clamp capacitor 42 which clamps outputs from the pixels 1, a MOS switch 43 for clamping an input potential of the gain amplifier 41, a clamp potential supply terminal 44 and a supply terminal 45 for supplying the gate of the clamp switch 43 with a switch pulse.

[0037]

Further, there are included a readout circuit (removing circuit) 22 which reads out a signal from the pixel 1, a capacitor 23 which holds the offset of the gain amplifier 41 at the time of outputting a signal based on the noise signal occurring when the potential of the pixels 1 is reset, a capacitor 24 which holds the offset of the gain amplifier 41 and the output of the gain amplifier 41, a switch MOS transistor 25 which controls conduction between the vertical output line 8 and the capacitor 23, a switch MOS transistor 26 which controls conduction between the vertical output line 8 and the capacitor 24, pulse supply terminals 37 and 38 which apply pulses to the gates of the switch MOS transistors 25 and 26, respectively, a horizontal output line 27 to which a signal held in the capacitor 23 is transmitted, a horizontal output line 28 to which an signal held in the capacitor 24 is transmitted, a switch MOS transistor 29 which controls conduction between the capacitor 23 and the horizontal output line 27 and a switch MOS transistor 30 which controls conduction between the capacitor 24 and the signal output line 28.

[0038]

In addition, there are included a horizontal output line reset MOS transistor 31 which resets the potential of the horizontal output line 27, a horizontal output line reset MOS transistor 32 which resets the potential of the horizontal

output line 28, a power supply terminal 33 which supplies a reset potential to the source electrodes of the horizontal output line reset MOS transistors 31 and 32, a horizontal scanning circuit 34 which sequentially selects the capacitors 23 and 24, a first column selection output line 35-1 and a second column selection output line 35-2 which transmit signals from the horizontal scanning circuit 34 to the switch MOS transistors 29 and 30, a pulse supply terminal 36 which applies a pulse to the gates of the horizontal output line reset MOS transistors 31 and 32, a differential amplifier 39 which amplifies and outputs the voltage difference between the potential of the horizontal output line 27 and that of the signal output line 28 and an output terminal 40 of the differential amplifier 39.

[0039]

Here, Figure 1 illustrates, for the sake of simplification, an appearance with the pixels 1 being arranged in 2 rows and 2 columns. However, in practice, the number of the pixels 1 will correspond with an intended use. In addition, the pixels 1 will not be limited to a matrix form arrangement but can be arranged in a delta form and a honeycomb form.

[0040]

Figure 2 is an equivalent circuit diagram of a gain amplifier 41 in Figure 1. Figure 2 includes a differential input stage 46, a non-inverting input part 47, an inverting input part 48, a constant current supply MOS transistor 49, a source follower 50 being an output stage, an output part 51, a constant current supply MOS transistor 52, connection 53 which connects the output part of the differential input stage 46 and the input part of the source follower 50, a MOS transistor 54 which connects the output part 51 to the inverting input part 48, a capacitor 55 having one electrode connected to an inverting input part 48 and the other electrode connected to the ground or to a fixed potential, a capacitor 56 having one electrode connected to an inverting input part 48 and the other electrode connected to the output part 51, a terminal 57 which supplies the gates of the MOS transistors 49 and 52 with constant potentials, and a terminal 58 which applies a control pulse to the gate of the MOS transistor 54.

[0041]

Here, the gain amplifier 41 is designed to present offset dispersion smaller than the reset dispersion of the pixel 1 and if the absolute value of the gain is larger than 1, the configuration thereof does not have to be limited to the one illustrated in Figure 2. For example, the differential input stage can be configured with another transistor and the source follower can be replaced by the emitter follower.

[0042]

As for offset, since the constraint on the layout of the gain amplifier 41 is generally more moderate than constraint on the layout of the pixel 1, it is sufficiently possible to design the gain amplifier with a small offset dispersion.

[0043]

In addition, by making the gain of the gain amplifier 41 larger than 1, signals output from the pixel 1 will finally be amplified by a factor of the gain. Accordingly, even if there is no change in noise of the differential amplifier 39 and thermal noise originated in the capacitors 23 and 24, the signal-to-noise ratio on random noise is improved.

[0044]

For comparison, the operation of the gain amplifier 41 illustrated in Figure 2 can be carried out at a constant current which does not depend on level of signal voltage. In addition, as described below, the gain can be set easily only by changing the capacitive dividing ratio of the capacitors 55 and 56, and therefore the gain amplifier is formed stably in general with the capacitive dividing ratio hardly incurring production dispersion, giving rise to an advantage that a constant gain is easily obtainable.

[0045]

If the current of the gain amplifier 41 depends on the signal voltage, a voltage drop amount originated in resistance of an earthing conductor and a power supply line for supplying the current to the gain amplifier 41 fluctuates and, therefore, offset level in the capacitors 23 and 24 are different and the difference thereof fluctuates based on the signal amount. Therefore, the offset removal rate drops so that the signal-to-noise ratio for the FPN drops. However, according to the gain amplifier 41, such a signal-to-noise ratio drop can be advantageously prevented.

[0046]

Figure 3 includes timing charts illustrating the operation of the circuit in Figure 1. Here, the MOS transistors illustrated in Figure 1 are all N types, which are turned on when the gate potential is at high level and off at low level.

[0047]

At first, when a pulse signal applied to the first row selection output line 18-1 by the vertical scanning circuit 17 is switched to high level, the operation of the pixels 1 on the first row will become feasible. When the pulse signal applied to the pulse terminal 16 is switched to high level, the source of the amplification MOS transistor 3 of the pixel 1 and the constant current supply MOS transistor 9 are brought into connection and the output of the signal from the side of the pixel 1 to the vertical output line 8 will become feasible.

[0048]

By switching the pulse signal applied to the pulse terminal 15 to high level, the reset MOS transistor 5 is turned on and the gate part of the amplification MOS transistor 3 is reset to a reset potential.

[0049]

Next, a pulse applied from the supply terminal 45 to the gate of the MOS transistor 43 is switched to high level. Moreover, a pulse applied to the pulse supply terminal 37 is switched to high level so that the input potential of the gain amplifier 41 is taken as the clamp potential.

[0050]

Here, the input part and the output part of the gain amplifier 41 are respectively the non-inverting input part 47 and the output part 51 in Figure 2.

[0051]

When the MOS switch 54 is turned on, the gain amplifier 41 operates as a voltage follower so that the inverting input part 48 is initialized. Therefore, by applying a pulse synchronized with the pulse applied to the supply terminal 45 to the supply terminal 58, the potential of the output part 51 is a sum of the offset voltage of the gain amplifier 41 and the potential of the non-inverting input part 47. The offset

of the gain amplifier 41 is stored in the capacitor 23.
[0052]

Next, by switching a pulse applied to the pulse terminal 14 to high level, optical signals generated in the photodiode 2 are transferred to the gate of the MOS transistor 3 through the transfer MOS transistor 4.
[0053]

Here, a noise signal occurring at the time of resetting the potential of the pixel 1 is superimposed onto the optical signal transferred to the gate of the MOS transistor 3.
[0054]

Subsequently, when a high level pulse is applied to the pulse supply terminal 38, an amplification signal based on an optical signal on which a noise signal is superimposed will be input to the gain amplifier 41. At that time, since the MOS switch 54 is turned off, that input signal serves as a voltage feedback operational amplifier and is amplified by a factor of the gain determined by the capacitive dividing ratio of the capacitors 55 and 56.
[0055]

Therefore, a signal is stored in the capacitor 24 subjected to superimposition of the offset level of the gain amplifier 41 onto the output signal of the gain amplifier. For comparison, with values of the capacitors 55 and 56 being C1 and C2 respectively, (C1+C2)/C2 will become the gain.
[0056]

When the horizontal scanning circuit 34 is driven, the pulse signals output to the first column selection output line 35-1 and a second column selection output line 35-2 sequentially get to high level. The signals stored in the capacitors 23 and 24 are output to the horizontal output lines 27 and 28 through the MOS transistors 29 and 30 respectively.
[0057]

Before the high level pulses are output to the first column selection output line 35-1 and the second column selection output line 35-2, it is necessary that the pulse applied to the pulse supply terminal 36 is set at high level to reset the potential of the horizontal output lines 27 and 28 through the horizontal output line reset MOS transistors 31 and 32 in advance.

[0058]

Respective signals lead to the horizontal output lines 27 and 28 are input to the differential amplifier 39 so that the difference is taken and the amplification signal based on an optical signal is output from the output terminal 40.

[0059]

Similarly, if signals are read out from the pixels 1 in the second row, amplification signals based on the optical signals are output from the output terminal 40.

[0060]

Thus, if clamping is carried out by the MOS switch 43 during the period when the noise signal of the pixel 1 is output to take the input potential of the gain amplifier 41 as the clamp potential, the offset of the gain amplifier 41 is removed by the differential amplifier 39 and finally a sensor signal with small offset dispersion is obtainable.

[0061]

(Embodiment 2)

Figure 4 is an equivalent circuit diagram of a solid-state image pickup apparatus of an embodiment 2 of the present invention. Figure 4 includes a readout circuit (removing circuit) 59 including a clamp circuit, a capacitor 60 for holding signals after clamping, a switch MOS transistor 61 which controls conduction between the clamp capacitor 42 and the capacitor 60, a horizontal output line 62 to which a signal held in the capacitor 60 is output, a MOS transistor 65 which resets the potential of the horizontal output line 62, an amplifier 66 which amplifies a signal transmitted through the horizontal output line 62 and an output terminal 67 of the amplifier 66. Here, in Figure 4, like reference numerals and characters designate the same or similar parts in Figure 1.

[0062]

Figure 5 includes timing charts illustrating the operation of the circuit in Figure 4. Here, the MOS transistors illustrated in Figure 4 are all N types, which are turned on when the gate potential is at high level and off at low level.

[0063]

At first, when a pulse signal applied to the first row selection output line 18-1 by the vertical scanning circuit 17

is switched to high level, the operation of the pixels 1 on the first row will become feasible. When the pulse signal applied to the pulse terminal 16 is switched to high level, the source of the amplification MOS transistor 3 of the pixel 1 and the constant current supply MOS transistor 9 are brought into connection and output of the signal from the side of the pixel 1 to the vertical output line 8 will become feasible.
[0064]

By switching the pulse signal applied to the pulse terminal 15 to high level, the reset MOS transistor 5 is turned on and the gate part of the amplification MOS transistor 3 is reset to a reset potential.
[0065]

Then, the amplification signal based on the noise signal occurring at the time of resetting is output from the pixels 1 to the vertical output line 8. That amplification signal is amplified by the gain amplifier 41.
[0066]

Thereafter, setting the pulse signal, which is input from the pulse input terminal 64, to high level and setting the pulse, which is applied to the supply terminal 45, to high level, the capacitor 60 will become the clamp potential supplied from the clamp potential supply terminal 44.
[0067]

Next, by switching a pulse applied to the pulse terminal 14 to high level, optical signals generated in the photodiode 2 are transferred to the gate of the MOS transistor 3 through the transfer MOS transistor 4.
[0068]

Then, the gate of the MOS transistor 3 is turned on so that an amplification signal based on an optical signal on which a noise signal is superimposed will be output from the pixels 1 and input to the gain amplifier 41.
[0069]

Consequently, the capacitor 60 will come into the state where a clamp potential is added to a potential based on the output signal of the gain amplifier 41. At that time point, the pulse signal applied to the pulse input terminal 64 is returned to low level. The signal stored in the capacitor 60 will become a signal not including the noise signal of the

pixels 1 and the offset of the gain amplifier 41 by the clamping operation.

[0070]

Thereafter, when the horizontal scanning circuit 34 is driven, the pulse signals output to the first column selection output line 35-1 and the second column selection output line 35-2 sequentially get to high level. The signals stored in the capacitor 60 in each of the pixels 1 are lead to the horizontal output line 62 through the MOS transistor 63 respectively.

[0071]

Before switching the pulse signals output to the first column selection output line 35-1 and the second column selection output line 35-2 sequentially to high level, it is necessary to reset the potential of the horizontal output lines 62 in advance likewise in the embodiment 1. Signal outputs lead to the horizontal output line 62 are input to the amplifier 66 so that the amplification signal based on an optical signal is output from the output terminal 67.

[0072]

Similarly, if signals are read out from the pixels 1 in the second row, amplification signals based on the optical signals are output from the output terminal 67.

[0073]

Here, voltage of the signal from the pixels 1 undergoes capacitive division twice, that is, capacitor split between the clamp capacitor 42 and the storage capacitor 60 and capacitive division between the capacitor 60 and the capacitor of the signal output line 62 and, however, is amplified by a factor of the gain by the gain amplifier 41. Therefore, the signal voltage at the time of being input to the amplifier 66 will not drop significantly.

[0074]

On the other hand, dispersion of the noise signal in the pixels 1 and offset dispersion in the gain amplifier 41 are removed by the clamp circuit. Therefore, high signal-to-noise ratio will be also attainable on the FPN and on the random noise.

[0075]

In addition, the input part capacitor of the gain

amplifier 41 in the present embodiment becomes sufficiently small and therefore, in practice, a signal output from an arbitrary pixel 1 can charge up only the capacitor of the vertical output line 8 so that the pixel output can be sped up.

[0076]

(Embodiment 3)

Figure 6 is an equivalent circuit diagram of a solid-state image pickup apparatus of an embodiment 3 of the present invention. Operations of the solid-state image pickup apparatus shown in Figure 6 are likewise the operations of the solid-state image pickup apparatus in Figure 1. However, since the solid-state image pickup apparatus of the present embodiment comprises no clamp circuit, a signal based on the noise signal of the pixel 1 in addition to the offset of the gain amplifier 41 are stored in the storage capacitor 23 and a signal based on the noise signal of the pixel 1 in addition to the offset of the gain amplifier 41 and the output signal of the gain amplifier 41 are stored in the storage capacitor 24.

[0077]

Therefore, in the output terminal 40 of the amplifier 39, there appears removal residual of the dispersion between the signal based on the noise signal of the pixel 1 and the offset of the gain amplifier 41 as fixed pattern noise. However, dispersion of the offset of the gain amplifier 41 is small and, therefore, therefore the problem is not so significant.

[0078]

In addition, the gain amplifier 41 amplifies signals at a gain larger than 1. Therefore, the signal-to-noise ratio of the present embodiment on FPN is improved and the signal-to-noise ratio on the random noise is also improved since a signal is amplified by a factor of the gain by the gain amplifier 41.

[0079]

In addition, likewise the embodiment 2, as for an output from the pixel 1, in practice, only the parasitic capacitor of the vertical output line 8 may be charged up to give rise to an effect that the pixel output can be sped up.

[0080]

So far, in each embodiment, a case where the pixel 1

carries out signal amplification with an MOS transistor has been described as an example. However, the signal amplification can be carried out with another transistor.
[0081]
(Embodiment 4)

Figure 7 is a block diagram illustrating a schematic configuration of an image pickup system of an embodiment 4 of the present invention. Figure 7 includes a barrier 1051 serving as the protection and main switch of a lens, a lens 1052 for forming an optical image of an object onto a solid-state image pickup apparatus 1054 described in the embodiments 1 to 3, an iris 1053 for changing the amount of light transmitted through the lens 1052, a solid-state image pickup apparatus 1054 for receiving the object image formed by the lens 1052 as an image signal, an image pickup signal processing circuit 1055 which carries out processing such as various kinds of correction and clamping on image signals output from the solid-state image pickup apparatus 1054, an A/D converter 1056 for performing analog-to-digital conversion of the image signal output from the solid-state image pickup apparatus 1054, a signal processing unit 1057 which variously corrects image data output from the A/D converter 1056 and compresses data, a timing generation unit 1058 which outputs various kinds of timing signals to the solid-state image pickup apparatus 1054, the image pickup signal processing circuit 1055, the A/D converter 1056 and the signal processing unit 1057, an entire control and arithmetic operation unit 1059 which performs various kinds of arithmetic operations and controlling the entire still video camera, a memory unit 1060 which temporarily stores the image data, a recording medium control interface (I/F) unit 1061 for recording/reading out on/from a recording medium, a detachable recording medium 1062 such as a semiconductor memory for recording or reading out image data and an external interface (I/F) unit 1063 for communicating with an external computer or the like.
[0082]

Next, the operation of the still video camera with the above-described configuration at the time of image-taking will be described. When the barrier 1051 is opened, the main power supply is turned on, the power supply of the control system is

turned on next, and moreover, the power supply of the image pickup system circuit such as the A/D converter 1056 is turned on.

[0083]

Then, in order to control the exposure amount, the entire control and arithmetic operation unit 1059 opens the aperture of the iris 1053. The signal output from the solid-state image pickup apparatus 1054 passes through the image pickup signal processing circuit 1055 and is then output to the A/D converter 1056.

[0084]

The A/D converter 1056 carries out A/D conversion on that signal which is output to the signal processing unit 1057. The entire control and arithmetic operation unit 1059 calculates exposure on the basis of the data via the signal processing unit 1057.

[0085]

Determining brightness according to a result of carrying out that light measurement, the entire control and arithmetic operation unit 1059 controls the iris according to the result.

[0086]

Next, on the basis of the signal output from the solid-state image pickup apparatus 1054, a high-frequency factor is extracted, and the distance to the object is calculated by the entire control and arithmetic operation unit 1059. Thereafter, the lens 1052 is driven, and it is determined whether an in-focus state is obtained or not. If the state is out of focus, the lens 1052 is driven again, and distance measurement is performed.

[0087]

After confirming the in-focus state, main exposure starts. When exposure is ended, the image signal output from the solid-state image pickup apparatus 1054 undergoes correction and the like in the image pickup signal processing circuit 1055 and, moreover, undergoes A/D conversion by the A/D converter 1056, passes through the signal processing unit 1057, and is stored in the memory unit 1060 by the entire control and arithmetic operation unit 1059.

[0088]

Thereafter, the data stored in the memory unit 1060 is

recorded on the detachable recording medium 1062 such as a semiconductor memory through the recording medium control I/F unit 1061 under the control of the entire control and arithmetic operation unit 1059. The data may be directly input to a computer or the like through the external I/F unit 1063 to process the image.

[0089]

[Advantages of the Invention]

As has been described above, according to the present invention, reduction in FPN and random noise will become feasible to enable improvement in the signal-to-noise ratio.

[Brief Description of the Drawings]

[Figure 1]

Figure 1 is an equivalent circuit diagram of a solid-state image pickup apparatus of an embodiment 1 of the present invention.

[Figure 2]

Figure 2 is an equivalent circuit diagram of a gain amplifier 41 in Figure 1.

[Figure 3]

Figure 3 includes timing charts illustrating the operation of the circuit in Figure 1.

[Figure 4]

Figure 4 is an equivalent circuit diagram of a solid-state image pickup apparatus of an embodiment 2 of the present invention.

[Figure 5]

Figure 5 includes timing charts illustrating the operation of the circuit in Figure 4.

[Figure 6]

Figure 6 is an equivalent circuit diagram of a solid-state image pickup apparatus of an embodiment 3 of the present invention.

[Figure 7]

Figure 7 is a block diagram illustrating a schematic configuration of a solid-state image pickup system of an embodiment 4 of the present invention.

[Figure 8]

Figure 8 is a circuit diagram illustrating a conventional CMOS image sensor.

[Figure 9]

Figure 9 includes timing charts illustrating the operation of the circuit in Figure 8.

[Description of the Symbols]

1 pixel
2 photodiode
3 MOS transistor
4 transfer MOS switch
5 reset MOS switch
6 power potential supply line
7 selection switch MOS switch
8 vertical output line
9 constant current supply MOS transistor
10 reset control line
11 transfer control line
12 selection control line
13 constant potential supply line
14 to 16 pulse terminal
17 vertical scanning circuit
18-1 first row selection output line
18-2 second row selection output line
19 to 21 switch MOS transistor
22 readout circuit
23, 24 capacitor
25, 26 switch MOS transistor
27, 28, 62 horizontal output line
30 switch MOS transistor
31, 32 horizontal output line reset MOS transistor
33 power supply terminal
34 horizontal scanning circuit
35-1 first column selection output line
35-2 second column selection output line
36 to 38 pulse supply terminal
39 differential amplifier
40 output terminal
41, 66 gain amplifier
42 clamp capacitor
43 MOS transistor
44 clamp potential supply terminal
45 supply terminal

46 differential input stage
47 non-inverting input part
48 inverting input part
49 MOS transistor
50 source follower
51 output part
52 MOS transistor
53 connection
54 MOS transistor
55, 56 capacitor
57, 58 terminal

Figure 7

1052 LENS

1053 IRIS

1054 SOLID-STATE IMAGE PICKUP APPARATUS

1055 IMAGE PICKUP SIGNAL PROCESSING CIRCUIT

1056 A/D CONVERTER

1057 SIGNAL PROCESSING UNIT

1058 TIMING GENERATION UNIT

1059 ENTIRE CONTROL AND ARITHMETIC OPERATION UNIT

1060 MEMORY UNIT

1061 RECORDING MEDIUM CONTROL I/F UNIT

1062 RECORDING MEDIUM

1063 EXTERNAL I/F UNIT

#1 COMPUTER

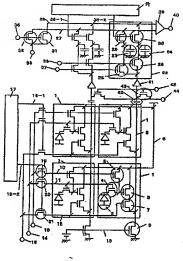
15

51 出力部
52 MOSトランジスタ
53 結線

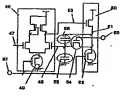
16

＊54 MOSトランジスタ
55, 58 容量
＊ 57, 58 端子

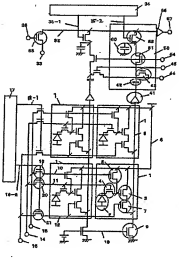
Fig. 1 【図1】



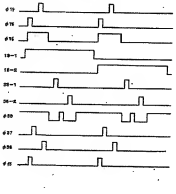
【図2】 Fig. 2



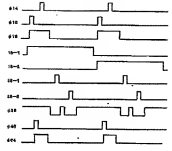
【図4】 Fig. 4



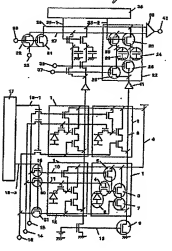
【図3】 Fig. 3



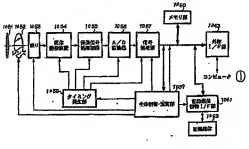
【図5】 Fig. 5



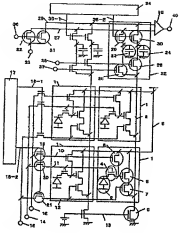
【図6】 Fig. 6



【図7】 Fig. 7



【図8】 Fig. 8



【図9】 Fig. 9